

MSOE EECS Department

CE-1900: Lab 4 Grading Checklist

Dr. Durant

Name: _____

Item	Points
Homework problems	/ 20
Truth table (page 5)	/ 15
VHDL File and appropriate documentation per example (no deduction for format & comments, this week only) Example: http://myweb.msoe.edu/ce1900/vhdl/hex7seg.vhd Use the example as a model; you do not need to document minterms, but document the goal and symbols produced by the architecture.	/ 15
Simulation – include all inputs and all outputs in TT order; count through minterms in TT order	/ 10
Explanation of Simulation – explain why your simulation indicates correct behavior given your design – i.e., illustrate that a few key columns give the correct output	/ 15
Demonstration (individual , due in lab week 5, late for partial credit)	/ 20
Hard copy of time log updated through the week that this lab assigned to be performed. Use this spreadsheet: http://myweb.msoe.edu/durant/courses/ce1900/timeLog.xlsx	/ 5
Total	/ 100

- **Staple** this lab cover sheet on top of all the materials you are submitting.
- Submit everything in the **order** listed above.
- You may omit pages from the lab packet that do not contain work you are submitting.
- Your lab packet is due by the end of the week 5 lab period. If you are unable to complete the demonstration during the week 5 lab period, you may wish to make copies of key pages before turning in your lab packet.
- Extra copies of lab checkout sheets are available on my CE1900 website.